

## PWM Sets Output of LCD/LED Driver

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The circuit consists simply of a PWM source, capacitor C, and resistors R<sub>D</sub> and R<sub>W</sub>. For CMOS outputs, you calculate the open-circuit output voltage as:

$$V_{\text{CONT}} = D \times V_{\text{DD}}$$

where D is the PWM duty cycle and V<sub>DD</sub> is the logic supply voltage. The control circuit's output impedance is the sum of resistor values R<sub>W</sub> and R<sub>D</sub>:

$$R_{\text{CONT}} = R_{\text{D}} + R_{\text{W}}$$

For the circuit of Figure 1, the output voltage (V<sub>OUT</sub>) is a function of the PWM average voltage (V<sub>CONT</sub>):

$$V_{\text{OUT}} = V_{\text{REF}} \times \left( 1 + \frac{R_1}{R_2} \right) + \frac{(V_{\text{REF}} - V_{\text{CONT}}) \times R_1}{R_{\text{CONT}}}$$

where V<sub>REF</sub> is the reference voltage at the feedback input.

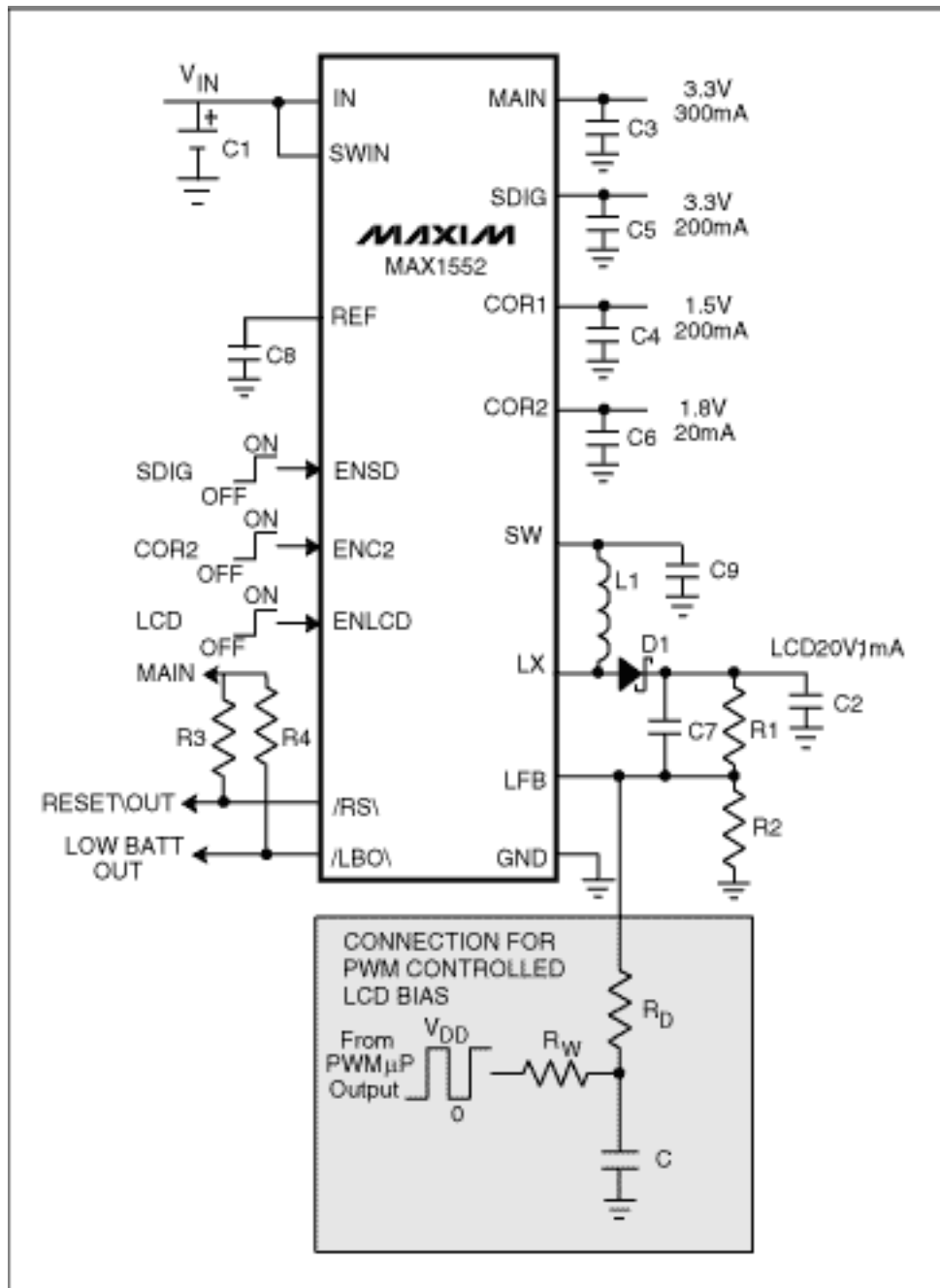


Figure 1. LCD Driver with positive output voltage.

Bear in mind that the initial charge on filter capacitor C produces a turn-on transient. The capacitor forms a time constant with  $R_{CONT}$ , which causes the output to initialize at a voltage higher than that intended. You can minimize this overshoot by scaling the value of  $R_D$  as high as possible with respect to  $R_1$  and  $R_2$ . As an alternative, the  $\mu P$  can disable the LCD until the PWM voltage stabilizes.

For Figure 2, the output voltage ( $V_{OUT}$ ) is a function of the PWM average voltage ( $V_{CONT}$ ):

$$V_{OUT} = V_{REF} + \frac{(V_{REF} - V_{CONT}) \times R_{FB}}{R_{CONT}}$$

where  $V_{REF}$  is the reference voltage at the feedback input.

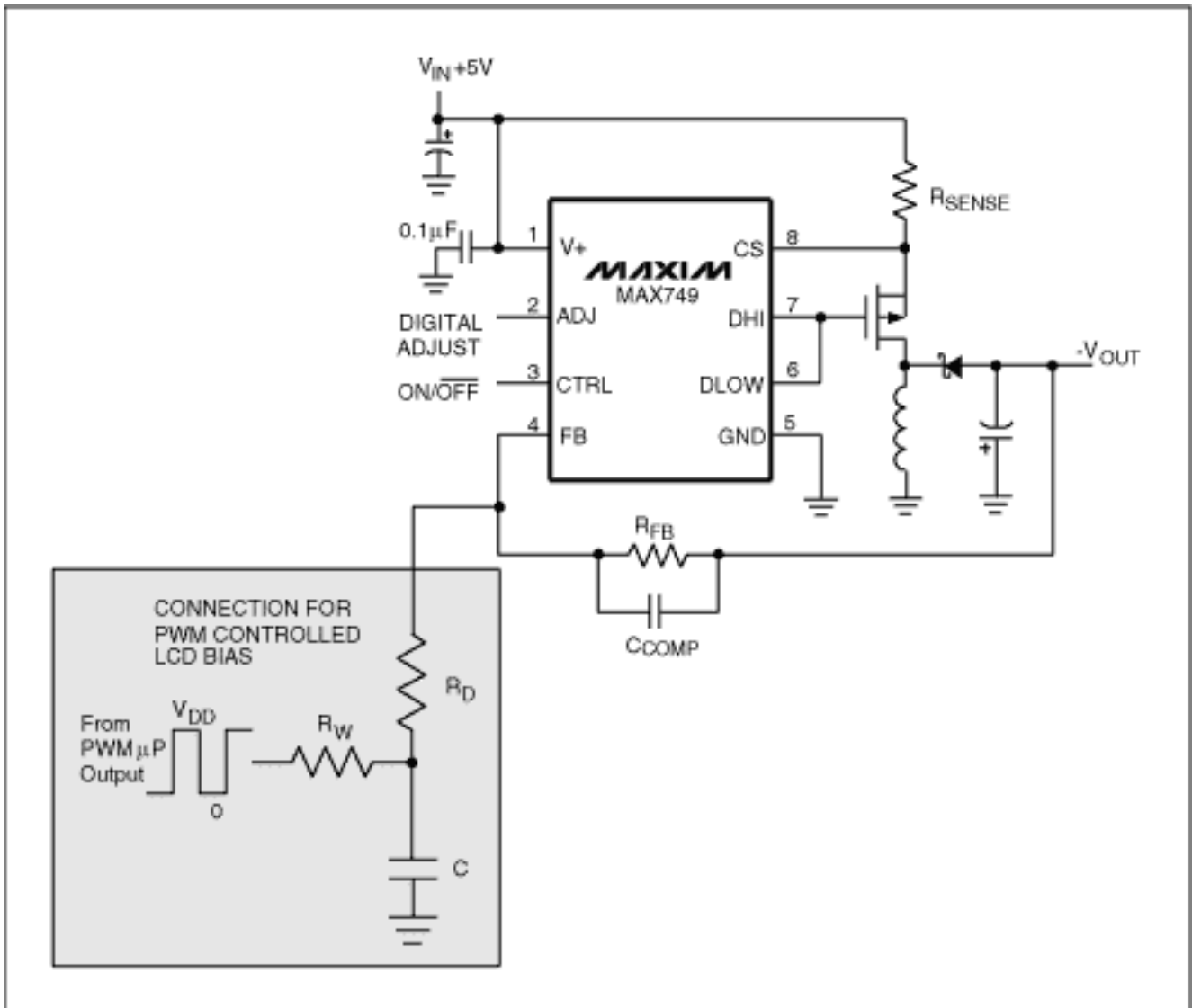


Figure 2. LCD driver with negative output voltage.

For Figure 3, the output current ( $I_{OUT}$ ) is a function of the PWM average voltage ( $V_{CONT}$ ):

$$I_{OUT} = \left[ \frac{V_{REF} + \frac{(V_{REF} - V_{CONT}) \times R_{SET}}{R_{CONT}}}{R_{SET}} \right] \times K$$

where  $V_{REF}$  is the reference voltage at the SET output and  $K$  is the current-scaling factor.

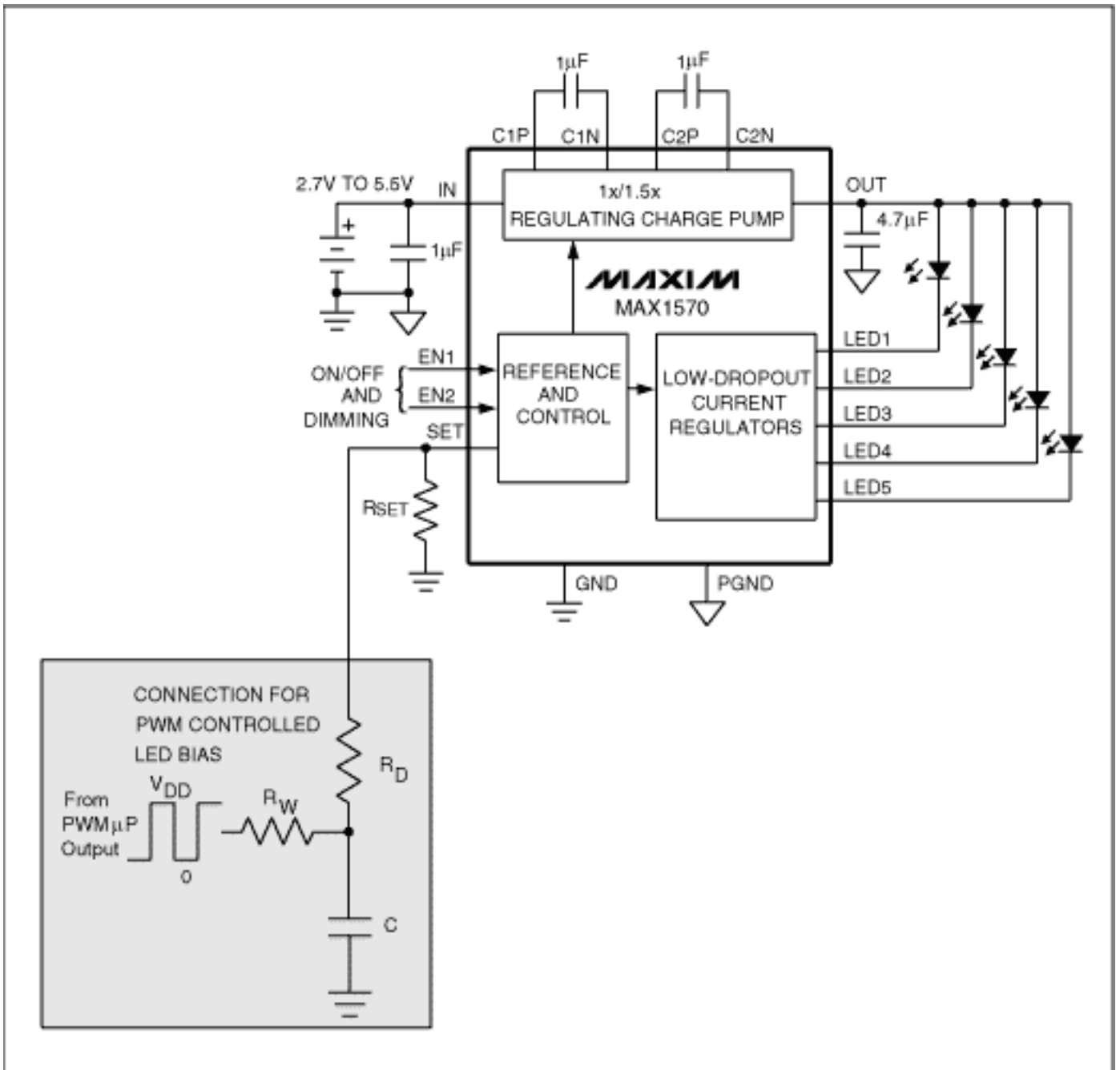


Figure 3. Current-controlled LED driver.

$R_D$  isolates the capacitor from the feedback loop in these PWM-adjustment methods. Assuming a stable voltage at the feedback point, the following equation defines the lowpass filter's cutoff frequency:

$$f_c = \frac{1}{2 \times \pi \times R \times C}$$

where  $R = R_W \parallel R_D$ . If  $R_D \gg R_W$ ,  $R \approx R_W$ . To minimize ripple voltage at the output, you should set the cutoff frequency at least two decades below the PWM frequency.

This design idea appeared in the May 27, 2004 issue of *ED* magazine.